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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,100	11/25/2003	Rainer Buchty	Buchty 1-7-1	9858

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LAW OFFICE OF JEFFREY M. WEINICK, LLC
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EXAMINER	
TSAI, SHENG JEN	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,100	BUCHTY ET AL.	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-18 and 26-32* is/are allowed.

6)☒ Claim(s) *1-9 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Request for Continued Examination (RCE) filed on February 2, 2007 regarding application 10,722,100 filed on November 25, 2003.

2. Claims 1 and 10 have been amended.

Claims 1-32 are pending for consideration.

3. ***Response to Amendments and Remarks***

Applicants' amendments and remarks have been fully and carefully considered, with the Examiner's response set forth below.

Upon further considerations, rejections of claims 10 and 26 under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Shahidzadeh et al. (US 6,349,380) have been withdrawn.

A new ground of claim analysis for claims 1-9 and 19-25 based on previously applied reference (Tanaka et al., US 4,910,667) has been made. Refer to the corresponding sections of the following claim analysis for details.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 7-9, 19-20, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667).

As to claim 1, Tanaka et al. disclose **a method** [Vector Processor with Vector Buffer Memory for Read or Write of Vector Data between Vector Storage and Operation Unit (title)] **for accessing at least one memory unit** [the corresponding memory unit including the main storage (figure 3, 96) and the vector buffer storage (figure 3, 21); figure 5 further shows the case where a plurality of vector buffer storages (221-1 and 221-2) are present] **based on an index vector comprising a plurality of values** [the corresponding index vector comprising Vector Base Registers (VB1, VB2 and VB3, figure 1, 12; figure 3, 108, 110 and 112), Vector Increment Registers (VI1, VI2 and VI3, figure 1, 13; figure 3, 109, 111 and 113), and Vector Length Registers (VL1, VL2 and VL3, figure 1, 11; figure 3, 11); refer to "Response to remarks on claim 1" presented earlier in this Office Action], **said method comprising the steps of**: **concurrently performing an operation on individual ones of said plurality of index vector values with a same base value to generate a plurality of memory addresses** [The content of the vector base register VBR selected from the group of registers 12 by the field R2 14-3 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l31. It indicates the start address of the vector data in the main storage. The content of the vector increment register VIR selected from the group of registers 13 by the field R3 14-4 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l32. It indicates the increment for the vector data. The start address and

the increment are keys to check whether the necessary vector data is stored in the vector buffer storage 21. In the present identification embodiment, the start address and the increment are used as the information to identify the vector data (column 4, lines 26-42); Note that 3 requestors (figure 3, 103, 104 and 105) are present to support concurrent operations of the 3 sets of Vector Base Registers and Vector Increment Registers]; **and**

concurrently accessing individual ones of said plurality of memory addresses in said at least one memory unit [Note that 3 requestors (figure 3, 103, 104 and 105) are present to support concurrent accessing of the 3 memory locations specified by the 3 sets of Vector Base Registers and Vector Increment Registers; the location of the vector data on the main storage 96 is designated by 108 and 113. The address of the two vector data to be read are designated by VB1 108, VI1 109, VB2 110 and VI2 111, where VB represents a start address of the vector data and VI represents an increment for the vector data. The address on the main storage of the vector data to be stored is designated by VB3 112 and VI3 113. The VB1 and VI1 are sent to the vector buffer storage control 102 and the fetch requestor 103. The VB2 and VI2 are sent to the vector buffer storage control 102 and the fetch requestor 104. The VB3 and VI3 are sent to the vector buffer storage control 103 and the store requestor 105 (column 7, lines 40-53)].

Regarding claim 1, Tanaka et al. do not explicitly teach that a same base value is used to concurrently perform an operation with the index vector values. Rather, Tanaka

et al. teach that an individual base value is used with a respective index vector value to concurrently perform an operation.

However, Tanaka et al. teach that each of the individual base value may assume a value from the same range of values. Since all individual base values may assume any value from the same range, it includes the cases where all individual base values assume the same value.

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to conclude, from the teaching from Tanaka et al., that since all individual base values may assume any value from the same range, it includes the cases where all individual base values assume the same value. Thus this particular limitation of claim 1 lacks patentable significance.

As to claim 2, Tanaka et al. teach that **said operation is addition** [The content of the vector base register VBR selected from the group of registers 12 by the field R2 14-3 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l31. It indicates the start address of the vector data in the main storage. The content of the vector increment register VIR selected from the group of registers 13 by the field R3 14-4 is sent to the vector buffer storage control 20, the fetch requestor 94 and the store requestor 95 through a line l32. It indicates the increment for the vector data. The start address and the increment are keys to check whether the necessary vector data is stored in the vector buffer storage 21. In the present identification embodiment, the start address and the increment are used as the

information to identify the vector data (column 4, lines 26-42). Note that "increment" means "addition"].

As to claim 7, Tanaka et al. teach that **at least one memory unit comprises a plurality of memory units** [the corresponding memory unit including the main storage (figure 3, 96) and the vector buffer storage (figure 3, 21); figure 5 further shows the case where a plurality of vector buffer storages (221-1 and 221-2) are present] **and wherein said step of concurrently accessing comprises the step of accessing individual ones of said plurality of memory addresses in one corresponding memory unit** [refer to "Response to remarks on claims 7 and 25" presented earlier in this Office Action; If the vector buffer storage control 20 determines that the desired vector data is in the vector buffer storage 21, it sends the address of the vector data and a read signal to the vector buffer storage 21 through a line l41, and sends a select signal through a line l39 so that the vector data is transferred from the vector buffer storage 21 to the vector registers 98 through the selector 71. If the vector buffer storage control 20 determines that the desired vector data is not in the vector buffer storage 21, it activates the fetch requestor 94 through a line l43 to send the vector data to the vector registers 98 from the main storage 96 through the storage control 97, a line l38 and the selector 71. The address of the vector data and a write signal are sent from the vector buffer storage control 20 through a line l42, and the vector data is written into the vector buffer storage 21 through a line l38 (column 4, lines 43-59)].

As to claim 8, Tanaka et al. teach that **the step of concurrently accessing further comprises the steps of:**

concurrently reading data [Read Control, figure 2, 68)] **from individual ones of said plurality of memory addresses** [Note that 3 requestors (figure 3, 103, 104 and 105) are present to support concurrent accessing of the 3 memory locations specified by the 3 sets of Vector Base Registers and Vector Increment Registers; the location of the vector data on the main storage 96 is designated by 108 and 113. The address of the two vector data to be read are designated by VB1 108, VI1 109, VB2 110 and VI2 111, where VB represents a start address of the vector data and VI represents an increment for the vector data. The address on the main storage of the vector data to be stored is designated by VB3 112 and VI3 113. The VB1 and VI1 are sent to the vector buffer storage control 102 and the fetch requestor 103. The VB2 and VI2 are sent to the vector buffer storage control 102 and the fetch requestor 104. The VB3 and VI3 are sent to the vector buffer storage control 103 and the store requestor 105 (column 7, lines 40-53)]; **and**

storing said data in a storage register [the corresponding storage register is the vector registers (figure 1, 98)]

As to claim 9, Tanaka et al. teach that **the step of concurrently accessing further comprises the step of concurrently writing data to individual ones of said plurality of memory addresses** [Write Control, figure 2, 69; Note that 3 requestors (figure 3, 103, 104 and 105) are present to support concurrent accessing of the 3 memory locations specified by the 3 sets of Vector Base Registers and Vector Increment Registers; the location of the vector data on the main storage 96 is designated by 108 and 113. The address of the two vector data to be read are

designated by VB1 108, VI1 109, VB2 110 and VI2 111, where VB represents a start address of the vector data and VI represents an increment for the vector data. The address on the main storage of the vector data to be stored is designated by VB3 112 and VI3 113. The VB1 and VI1 are sent to the vector buffer storage control 102 and the fetch requestor 103. The VB2 and VI2 are sent to the vector buffer storage control 102 and the fetch requestor 104. The VB3 and VI3 are sent to the vector buffer storage control 103 and the store requestor 105 (column 7, lines 40-53)].

As to claim 19, refer to "As to claim 1" presented earlier in this Office Action.

As to claim 20, refer to "As to claim 1" presented earlier in this Office Action.

As to claim 25, refer to "As to claim 7" presented earlier in this Office Action.

6. Claims 3 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Matsugami et al. (US 5,929,928).

As to claims 3 and 21, Tanaka et al. do not teach that said operation is bit replacement.

However, Matsugami et al. teach in their invention "Digital Image Processor" a method and apparatus of accessing image memory [figure 6] where a "Bit Replacement Circuit" [figure 11, 54] is used [column 9, lines 21-60].

The use of a bit replacement circuit allows the direct substitution of all or portion of a bit pattern to generate a new bit pattern, and is usually faster than other operations such as addition or Boolean operations [column 9, lines 21-60].

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using a bit replacement circuit, as

demonstrated by Matsugami et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the performance of the system.

7. Claims 3-5 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Lavelle et al. (US 5,649,142).

As to claims 3-5 and 21-23, Tanaka et al. do not teach **the bit replacement operations as recited in the claims**.

However, Lavelle et al. teach in their invention "Method and Apparatus for Translating Addresses Using Mask and Replacement Value Registers and for Accessing a Service Routine in Response to a Page Fault" a method and apparatus of translating a first address in a first address space to a second address in a second address space [abstract; figure 4] where a "Bit Replacement Circuit" [figure 4, 406, 408, 412, 414, 418, 420 and 422] including a "0-20 bit replacement value" [figure 4, 418] is used to replace the least significant bits [bits 0-20] of a 32-bit virtual address [figure 4, 402] to generate a 32-bit physical address [figure 4, 422]. Note the inclusion of the "compare address for page match determination" unit [figure 4, 414], which facilitates the detection of a particular address pattern, such as all 0's, that would be present in bits 0-20. Also note that the 32-bit address is formed by concatenating bits 0-20 [figure 4, 418] and bits 21-32 [bit offset, figure 4, 420].

The use of a bit replacement circuit is vital in supporting single-instruction, multiple-data (SIMD) architecture in which multiple processor units executing the same instruction on a plurality of data, as the addresses of the plurality of data must be generated efficiently [column 1, lines 21-67].

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using a bit replacement circuit in support of a SIMD environment, as demonstrated by Lavelle et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the performance of the system.

8. Claims 6 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US 4,910,667), and in view of Gurney et al. (US 6,745,315).

As to claims 6 and 24, Tanaka et al. do not teach that **the memory unit comprises a multiport memory unit**.

However, Gurney et al. teach in their invention "Generation of Address Pattern through Employment of One or More Parameters to Store Information at Parts of Storage That Are Employable with Multiprocessor" a method and apparatus of generating address pattern [abstract; figures 2-3] where a plurality of dual port memory units are employed [figure 3, 760] from which vector data is generated [figures 8 and 10].

The use of multiport memory units allows the simultaneous accessing via the two ports by two processors, hence increasing the throughput of the system.

Therefore, it would have been obvious for one of ordinary skills at the time of Applicants' invention to recognize the benefits of using multiport memory units in support of a multi-processor environment, as demonstrated by Gurney et al., and to incorporate it into the existing apparatus disclosed by Tanaka et al. to further improve the throughput of the system.

9. ***Allowable Subject Matter***

10. Claims 10-18 and 26-32 are allowed.

11. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Kashiyama et al., (US 5,247,695), "Vector Processor with Byte Access of Memory."
- Omoda et al., (US 4,677,547), "Vector Processor."
- Takamine et al., (US 4,811,213), "Vector Processor with Vector Registers."
- Aoyama et al., (US 4,991,083), "Method and system for extending Address Space for Vector Processing."
- Kinoshita, (US 5,887,182), "Multiprocessor System with Vector Pipelines."
- Cray, Jr., (US 4,128,880), "Computer Vector Register Processing."
- Yokoyama, (US 5,136,699), "Logical Address Generating Device for an Instruction Specifying Two Words, each Divided into Two Parts."
- Fujii et al., (US 5,437,043), "Information Processing Apparatus Having a Register File Used Interchangeable Both as Scalar Registers of Register Windows and as vector Registers."
- Mishina et al., (US 5,010,483), "Vector Processor Capable of Indirect Addressing."
- Omoda et al., (US 4,825,361), "Vector Processor for Reordering Vector Data During Transfer from Main Memory to Vector Registers."

- Potash et al., (US 4,760,518), "Bi-Directional Databus System for Supporting Superposition of Vector and Scalar Operations in a Computer."

Conclusion

12. Claims 1-9 and 19-25 are rejected as explained above.

Claims 10-18 and 26-32 are allowed.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

March 6, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
3/9/07